internal address.

REMARKS

The Applicant has carefully reviewed and considered the Office Action mailed on February 13, 2001, and the references cited therewith. Claims 13, 15, 16, 20 and 21 are amended, no claims are canceled, and claims 62-71 have been added. As a result, claims 11-21 and 59-71 are now pending in this application.

Claim Objections

In §4 of the Office Action, claims 11 and 59-61 were objected to under 37 C.F.R. 1.75(b) as not substantially differing from each other. The Applicant respectfully submits that claims 11 and 59-61 are clearly different from each other. In particular, claim 59 requires "a memory array", in addition to the "control logic" and "switching circuitry" recited by claim 11. Claim 59 further specifies that the memory array is accessed in an unpatterned fashion for pipelined access, and a patterned fashion for burst data access (neither of which is specified by claim 11). Claim 60 recites a memory array which is "operable in a burst or pipeline mode of operation," without specifying whether the pipeline/burst modes are patterned or unpatterned. Finally, claim 61 is directed even more narrowly, to a dynamic random access memory, which is not recited by any of claims 11, 59, or 60. None of these elements is the same as the others; each has a clearly defined difference according to the recited elements.

For example, the storage device of claim 11 does not include a memory array that is operatively connected to the control logic (as does claim 59), or a memory array operable in burst/pipeline modes (as does claim 60). Nor is the storage device of claim 11 specified to be a dynamic random access memory (see claim 61). Moreover, the memory device of claim 59 includes control logic to select between unpatterned pipeline and patterned burst data patterns (not recited by claims 60-61). Finally, the memory device of claim 60 includes at least one memory array, while the dynamic random access memory of claim 61 includes more than one memory array. Clearly, requiring a memory array to be connected to the control logic, reciting a particular type of pipeline/burst data pattern, requiring the memory array to operate in burst/pipeline modes, and including a plurality of memory arrays in a dynamic random access

memory device are all substantially different elements. Thus, withdrawal of this objection is respectfully requested.

§102 Rejection of the Claims

In §6 of the Office Action, claims 11-21 and 59-61were rejected under 35 U.S.C. § 102(b) as being anticipated by Manning (U.S. Patent No. 5,652,724). The M.P.E.P. requires that "[t]he identical invention must be shown in as complete detail as is contained in the ... claim." *See* M.P.E.P. § 2131. Thus, the Applicant asserts that the Office has failed to show that Manning discusses the identical invention claimed in the instant application, and respectfully traverses the rejection by the Office.

The Applicant is unable to find, and the Office fails to show, where Manning discusses subject matter involving "switching circuitry for switching between a first pathway and a second pathway" which depends upon whether a patternless or a patterned addressing scheme is selected. For example, respecting claim 11, the Office asserts that the "patternless addressing scheme" of the Applicant's application is disclosed by the data output buffer having a two stage pipelined mode of operation disclosed by Manning at column 3, lines 27-28. The Office further notes that "Internal address generation with a pipelined data output provides for faster data access...." See Manning at column 3, lines 40-43. However, the M.P.E.P. requires that "... [d]uring patent examination, the pending claims must be 'given the broadest reasonable interpretation consistent with the specification.'" See M.P.E.P. § 2111. The Applicant respectfully submits that the assertion of the Office is inconsistent with the Applicant's specification, which teaches how to switch between pathways depending on whether the patternless or patterned addressing schemes are selected.

Manning teaches a burst EDO memory device having a pipelined output (i.e. read) buffer. See the Title of Manning. It is unreasonable to equate the pipelined output buffer of Manning with the patternless addressing scheme of the Applicant's invention. This becomes apparent when considering Manning's statement that "Internal address generation with a pipelined data output provides for faster data access ...". See Manning, above. If Manning teaches internal address generation as coexisting with pipelined data output, then there is apparently no need to switch between pathways, *as claimed* by the Applicant. Manning does indeed indicate that the

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ability "to switch between a standard non-burst mode and a high speed burst mode allows the device to be used to replace standard devices." See Manning at column 3, lines 37-39. However, Manning fails to discuss how to switch between pathways based on the selection of patternless/patterned addressing schemes.

The Office also cites Manning, with respect to claim 20, as disclosing a "... patternless addressing scheme ... for a random CAS" at column 3 lines 28-30 and 40-43, the Applicant can find no mention of this use of the /CAS line; rather, the discussion merely relates to /CAS line clocking and loading. Further, while the Office cites Manning as disclosing a "... a patterned addressing scheme ... for [a] sequence[d] CAS" in Fig. 1, refs. 26 and 30 and at column 7 line 35, the Applicant can find no mention of this use of the /CAS line; rather, the discussion merely relates to the general concept of "address sequences" for the /CAS line, and not to whether such sequences are patterned, or otherwise.

Thus, regarding claims 11 and 59-61, and all claims depending therefrom, the Office cites Manning at Figure 1; column 3, lines 27-45; column 7, lines 35-64, and column 10, lines 65+ (which merely discusses burst/normal EDO modes of operation). The Applicant fails to find where Manning discusses switching between pathways based upon the selection of patternless/patterned addressing schemes. The Office also fails to show with any particularity which components of Figure 1 allegedly comprise the switching circuitry *as claimed* by the Applicant.

In short, what Manning discusses is not identical to the subject matter of applicants' invention, and therefore, the rejection is improper. The Applicant respectfully requests the rejection be withdrawn, along with reconsideration and allowance of claims 11-21 and 59-61.

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CONCLUSION

Claims 11-21 and 59-61 should now be in condition for allowance. The Office is respectfully requested to note that the Applicant has amended claims 13, 15, 16, 20, and 21 to correct typographical errors and to provide a proper antecedent basis for each element of the claims. Newly added claims 62-71 read on pending claims 11 and 60, and thus, should also be in condition for allowance.

The Applicant's representative has reviewed the other art made of record by the Office, but believes that the cited art is more pertinent to the instant application. Thus, the Applicant respectfully submits that all pending claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone the Applicant's attorney at (612) 373-6913 to facilitate prosecution of this application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 14 day of May, 2001.

Tina Pugh
Name

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Signature

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